WHAT IS CLAIMED IS:

1. A method of testing a level of ion implantation energy in ion implantation equipment, comprising:

implanting first conductive ions to a first depth in a semiconductor substrate to form a first well of the first and conductive ions in the semiconductor substrate;

implanting second conductive ions to a second depth, different from said first depth, in said semiconductor substrate to form a second well of the second conductive ions in the semiconductor substrate,

the second conductive ions having a valence different from that of the first conductive ions, and the implanting of said first and second conductive ions being carried out at the same region of the substrate such that the first and second wells constitute a well within a well wherein the wells overlap beginning at a boundary within said substrate;

subsequently measuring the sheet resistance of the semiconductor substrate; and

correlating the value of the sheet resistance to the level of ion implantation energy used in said forming of the wells.

2. A method of testing a level of ion implantation energy in ion implantation equipment, comprising:

performing a first ion implantation process in which first conductive ions are implanted to a first depth in at least one semiconductor substrate to form a first well

in each at least one semiconductor substrate;

performing a second ion implantation process in which second conductive ions are implanted into said semiconductor substrate to form a second well in each at least one semiconductor substrate,

the second conductive ions having a valence different from that of the first conductive ions,

the implanting of said second conductive ions being carried out at the same region of the substrate as said first conductive ions, such that the first and second wells constitute a well within a well wherein the wells overlap beginning at a boundary within said substrate, and

for at least one said substrate so specified, said second ion implantation process being carried out while varying the ion implantation energy such that a boundary region within the substrate where the first and second wells overlap contains a plurality of depth-wise locations where the resistance varies;

subsequently measuring the sheet resistance of said at least one semiconductor substrate to yield at least one sheet resistance value; and

correlating the at least one sheet resistance value to a level of ion implantation energy used in said forming of the wells.

3. The method as claimed in 2, wherein said first ion implantation process comprises forming a said first well on each of a plurality of semiconductor substrates using different ion implantation apparatuses, respectively, set to the same level of ion implantation energy, and said second ion implantation process comprises forming a

said second well on each of the semiconductor substrates using one of the implantation apparatuses, while varying the ion implantation energy ouput by the one of the ion implantation apparatuses.

4. The method as claimed in 2, wherein said first ion implantation process comprises forming a said first well on each of a plurality of semiconductor substrates using different ion implantation apparatuses, respectively, set to the same level of ion implantation energy, and said second ion implantation process comprises forming a said second well on each of the semiconductor substrates using the corresponding ion implantation apparatuses, respectively, while varying the ion implantation energy ouput by each of the ion implantation apparatuses.

5. The method as claimed in 3, and further comprising comparing ion implantation energy levels of the respective ion implantation apparatuses derived from the sheet resistance values measured for each of the semiconductor substrates.

6. The method as claimed in 4, and further comprising comparing ion implantation energy levels of the respective ion implantation apparatuses derived from the sheet resistance values measured for each of the semiconductor substrates.

7. The method as claimed in 2, wherein said second implantation process comprises initiating the second process at set level of ion implantation energy, and varying the level of ion implantation energy within a range of 0.5 ~ 8% of the initial

set level of ion implantation energy.

8. The method as claimed in 2, wherein each said at least one semiconductor substrate is doped with a p-type impurity, and one of said first and second implantation processes comprises doping each said at least one substrate with an n-type impurity, and the other of said first and second ion implantation processes comprises doping each said at least one substrate with a p-type impurity to a depth less than the depth to which the substrate was doped with the n-type impurity, whereby a p-well is formed within and at the top of an n-well in each said at least one substrate.